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Design and Characterization of a 0.9-V Differential Inverter-Based OTA

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Most consumer electronics related electronic devices are battery powered, so reducing power consumption is a key objective in today's electronic circuit design. However, there are challenges in the design of electronic circuits, such as maintaining the performance of analog circuits within successive reductions in supply voltages. Amplifiers based on inverters have several features for designing integrated circuits, as they have higher transconductance efficiency compared to conventional OTAs (Operational Transconductance Amplifiers). In this way, the CMOS transistors used in these circuits operate with low supply voltage and low power consumption. A recurring problem of inverter-based OTAs is their unstable common mode voltage. A strategy to overcome this problem is the use of current sources to bias the transistors. Thus, their currents are dependent on the common-mode feedback circuit.

The topology designed and analyzed in this work is an inverter-based OTA with two control transistors. This OTA is designed with a reduced supply voltage of 0.9V on a 180nm CMOS technology. The control voltage (Vctrl) is generated by the common mode feedback circuit (CMFB). The Vctrl signal is refined to maintain operation in the desired VDD/2 region also for the common mode voltage (Vcm). A differential amplifier is introduced to establish the Vctrl value in order to support variations in PVT (process, voltage and temperature) and to reduce the need of regulators that impair the accuracy of the circuit, where a common mode voltage (Vcm) input forces a control voltage (Vctrl) to VDD/2. The circuit compares the OTA Von and Vop output signals (negative and positive output) with the common mode voltage and generates an error signal (Vctrl) which is fed back to the OTA, thus keeping the circuit stable to variations. Initially, the output common-mode voltage level was set to VDD/2.

The channel length of the transistors was fixed at 1 µm and the channel width for all NMOS transistors was kept fixed at 2 µm in the OTA and CMFB circuits. However, the width of the PMOS transistors was varied so that the output signal could operate in the desired range, with the number of multipliers (fingers) set to 70 on all transistors. From analyzes varying the width of the PMOS, the most accurate value to obtain the expected output signal was 15.7µm. With the sized OTA, the operation verification is performed through the CMFB. In this circuit, the width of the PMOS transistors was 14.0µm, thus obtaining the best operational performance so that the output signal reaches a voltage level of VDD/2.

The designed OTA was simulated at nominal temperature (27°C), with the circuit in open loop and with a balanced capacitive load of 10 pF, with a supply voltage of 0.9V. This OTA achieves a DC gain of 52.22dB and provides a GBW (gain bandwidth product) of

36.66MHz with a phase margin of 71.79º. The total current drawn by this circuit is 226.34μA leading to a power consumption of 212.7μW. The simulation that presents the rate of variation (Slew-Rate), where resistances are added to the feedback and OTA input, with resistances of 1 MΩ, presented in the positive ramp 0.37 V/μs and for the negative ramp 0.36 V/μs with total power consumption at 203.71 μW, the average rate of change of rise and fall time is close to 369 V/ms. Varying the temperature at -25ºC, 27ºC and 85°C, the OTA showed a small change in the DC voltage gain and in the phase margin, but the GBW is highly affected due to the fact that the GBW is proportional to the transconductance, so it increases with increasing temperature.

The Monte Carlo simulation calculates the circuit performance when undergoing processing and matching variations through random sampling, being performed with 500 runs. The average of the DC gain and the standard deviation are 52.15 dB and 91.76 mdB, respectively, where it is possible to verify a stable DC gain while the GBW is highly dependent on the process variations, so it is important to guarantee a safety margin during the design phase to meet project requirements.

Finally, this work presented the results of the design, characterization and simulation of a transconductance operational amplifier based on a self-biased inverter for sub-1V applications in 180nm CMOS technology. A CMFB circuit is used to control the common mode voltage at the outputs and attenuate the error signal. As transistors operate in weak inversion, good energy efficiency was obtained. Therefore, the performance of the OTA designed is suitable for data converters and analog filter applications.

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Keywords: OTA inverter; differential amplifier; self-bias; low power; transconductance.